REMARKS

In the Office Action dated October 22, 2003, claims 19-36 are pending, claims 19-33 and 36 are rejected and objections are made to claims 34 and 35. Applicants appreciate the indication of allowable subject matter, at least in claims 34 and 35.

Amended claim 19 is a combination of the pending claims 19 and 20.

New claims 37 and 38 correspond to the pending claims 34 and 35 rewritten in independent form. Thus, claims 37 and 38 should be allowable in view of the indication of allowability in the office action.

Objection to the specification is made for lack of section headings. This application is a 371 of an International application filed under the PCT. Thus, suggested subject headings are not required. However, if the Examiner desires, an amended specification will be submitted by Applicants.

Objection is made to the Abstract because "(Fig. 2)" should be deleted. In the amendment above, this objectionable term is deleted. A new page for the Abstract also is enclosed.

Objection is made to the drawings because Figure 5 should be designated by the legend "Prior Art". An amendment to Figure 5, as requested by the examiner, is proposed above and a new sheet of drawings including the amendment is enclosed.

Claims 19-33 are rejected under 35 U.S.C. §103(a) over Meyer, et al. (GB 2,139,128) in view of Yukutake et al (US 5,523,713).

The Examiner states that Meyer (GB 2,139,128) discloses

> in Fig. 6 an improved CMOS transmission gate circuit 50 comprising two cascaded transmission gates 52 and 54 with an earthing NMOS switch 56 (bypass circuit) connected to the middle node. Herein the switch 56 acts as a mechanism to reduce injection currents in the cell and to

> prevent noise on the other channels of the multiplexer (a bypass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate). Further, shown in Fig. 6, the switch 56 is controlled by the select signal SEL (multiplexer circuit further comprising a control circuit for controlling the bypass channel).

Applicant strongly disagrees with the understanding that Meyer teaches or suggests the present invention, whether or not combined with Yukutake.

For example, Meyer ***fails*** to teach or suggest a multiplexer circuit wherein a control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel. The switch 56 in the GB 2,139,128 is controlled by the **same** signal (Sel) **as the transistors** (58, 62) of the transmission gates (52, 54) (see page 6 lines 31-32, page 7 lines 13-14, 21-22, and 27-28; Fig. 6), i.e. depending on whether a signal at the input of transmission cell (50) shall be transferred to the output or not (page 8 lines 12-20), and not depending on a voltage in the input channel.

In the present application, however, a voltage in the input channel, i.e. in the path between the corresponding input (IN0 or IN1) and the output (OUT) is sensed (e.g. at point 70, 71 in Fig. 2), and depending on the value of this voltage, a by-pass circuit is controlled (page 7, first full paragraph to page 8 penultimate paragraph).

Applicants submit that Meyer ***fails*** to teach or suggest controlling a bypass circuit depending on a voltage in the input channel, as claimed in the present application.

Yukutake is cited for its disclosure of a multiplexer circuit comprising two input channels. Yukutake ***fails*** to make up for the deficiencies of Meyer. It also fails to teach or suggest controlling a bypass circuit depending on a voltage in the input channel, as claimed in the present application.

Thus, it is not seen how the present invention would have been obvious to one

of ordinary skill from any combination of the teachings of Meyer and Yukutake. Claims 21 - 36 also are patentable for at least the reasons discussed above.

In view of the discussion above, it is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

If for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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Abstract Of The Disclosure

A multiplexer circuit (100) comprises at least two input channels (IN_0, IN_1) and an output channel (2), each input channel (IN_0, IN_1) comprising a first transmission gate (FT_0, FT_1) which can be switched by a select signal ($SELECT_0$, $\overline{SELECT_0}$; $SELECT_1$, $\overline{SELECT_1}$) for connecting the input channel (IN_0, IN_1) to the output channel (2), and wherein at least one of the input channels (IN_0, IN_1) comprises a bypass circuit for preventing a current flowing through the first transmission gate (FT_0, FT_1) from reaching the other input channel, and a second transmission gate (ST_0, ST_1).